I Claim:

1. A configurable parameter estimator for a pilot channel, the parameter estimator comprising:

an open-loop channel estimator for performing an open-loop phase estimation;

a first filter coupled to the parameter estimator, the first filter for integrating a first signal from the open-loop channel estimator; and

a second filter coupled to the parameter estimator, the second filter for integrating a second signal from the open-loop channel estimator, the first filter and the second filter providing an error-correcting signal.

2. The configurable parameter estimator recited in Claim 1 wherein the open-loop channel estimator further comprises:

a first interface for providing an in-phase portion and a quadrature-phase portion of a first pilot demodulated sequence;

a second interface for providing the in-phase portion and the quadrature-phase portion of a second pilot demodulated sequence;

a first adder coupled to the first interface and the second separator, the first adder for adding the in-phase portion of the first pilot demodulated sequence and the quadrature-phase portion of the second pilot demodulated sequence; and

a second adder coupled to the first interface and the second separator, the second adder for subtracting the quadrature-phase portion of the first pilot demodulated sequence from the in-phase portion of the second pilot demodulated sequence.

3. The configurable parameter estimator recited in claim 1 wherein the first filter and the second filter are a finite impulse response (FIR) that produce an in-phase correction sample and a quadrature-phase correction sample, respectively.

4. The configurable parameter estimator recited in claim 1 wherein the first filter and the second filter have a variable pilot filter length.

5. The configurable parameter estimator recited in Claim 2 further comprising:

a multiplier coupled to the first separator, the multiplier for multiplying a pilot code times the in-phase portion of the code-demodulated sample to create the first pilot demodulated sequence.

6. The configurable parameter estimator recited in Claim 2 further comprising:

a multiplier coupled to the second separator, the multiplier for multiplying a pilot code times a quadrature-phase portion of the code-demodulated sample to create the second pilot demodulated sequence.

7. An electronic device for correcting the phase of a data signal, the electronic device comprising:

a first input for receiving a phase correction signal;

a second input for receiving the data signal; and

a multiplier coupled to the first input and the second input, the multiplier multiplying the phase correction signal with the data signal to produce a phase-corrected data signal.

8. The electronic device recited in Claim 7 further comprising:

an interface coupled to the multiplier, the interface for communicating a real signal corresponding to an m-ary phase.

9. The electronic device recited in Claim 7 further comprising:

a delay device coupled to the first input and the multiplier, the delay device for delaying the data signal.

10. The electronic device recited in Claim 7 further comprising:

a compare circuit coupled to the delay device, a compare circuit for comparing a desired delay with an actual delay, the compare circuit providing a dump enable signal to the delay device.

11. The electronic device recited in Claim 7 wherein the multiplier has complex multiply components for m-ary phase signal components.

12. A configurable demodulator for demodulating a user code from a received signal, the configurable demodulator comprising:

a first multiply-logic device for multiplying a first product code with an encoded data signal to produce a first code demodulated chip sequence, the first product code including at least a user code sequence;

a first accumulator coupled to the first multiply-logic device, the first accumulator summing the first code demodulated chip sequence to produce a first code-demodulated sample;

a second multiply-logic device for multiplying a second product code with the encoded data signal to produce a second code demodulated chip sequence, the second product code including at least a user code sequence; and

a second accumulator coupled to the second multiply-logic device, the second accumulator summing the second code demodulated chip sequence to produce a second code-demodulated sample.

13. The configurable demodulator recited in Claim 12 wherein the first product code includes the user code sequence and an in-phase portion of an extended code sequence, and wherein the second product code includes the user code sequence and a quadrature-phase portion of the extended code sequence.

14. The configurable demodulator recited in Claim 12 further comprising:

a compare circuit coupled to the first accumulator and the second accumulator, the compare circuit for comparing a desired integration length to a current integration length, the compare circuit providing a dump enable signal to the first accumulator and the second accumulator.

15. The configurable demodulator recited in Claim 12 wherein the first multiply-logic device and the second multiply-logic device each include complex multiply devices for a complex multiply operation.

16. The configurable demodulator recited in Claim 12 wherein the first accumulator and the second accumulator each have separate add-logic devices for adding an in-phase portion and a quadrature-phase portion of a signal.

17. A configurable demodulator for demodulating a traffic channel from a received signal, the configurable demodulator comprising:

a first multiplier for multiplying a traffic code sequence with a first received demodulated sample of the received signal to produce a first demodulated data sequence;

a first accumulator coupled to a first multiply-logic device, a first accumulator summing the first demodulated data chip sequence to produce a first intermediate demodulated output data sample;

a second multiplier for multiplying the traffic code sequence with a second intermediate code demodulated sequence to produce a second intermediate code demodulated sample; and

a second accumulator coupled to the second multiplier-logic device, the second accumulator summing the second intermediate code demodulated sequence to produce the second code-demodulated sample.

18. The configurable demodulator recited in Claim 17 further comprising:

a first adder coupled to the first accumulator and the second accumulator, the first adder for adding an in-phase component from the first accumulator to a quadrature-phase component from the second accumulator.

19. The configurable demodulator recited in Claim 17 wherein the first multiplier and the second multiplier each include complex multiply components for m-ary phase signal components.

20. The configurable demodulator recited in Claim 17 further comprising:

a compare circuit coupled to the first accumulator and the second accumulator, the compare circuit for comparing an input integration length to a current integration length, the compare circuit providing a dump enable signal to the first accumulator and the second accumulator.

21. A configurable digital coherent demodulator system for demodulating a digital signal, the digital coherent configurable demodulator system comprising:

a configurable traffic channel demodulator for demodulating a baseline channel into a traffic signal; and

a configurable correction device coupled to the configurable traffic channel demodulator, the configurable correction device having a complex multiplier for multiplying the traffic channel with a feed forward phase error correction signal.

22. The configurable digital coherent demodulator system recited in Claim 21 further compromising:

a configurable parameter estimator coupled to the configurable traffic channel demodulator and the configurable correction device, the configurable parameter estimator providing an error estimate of a pilot channel.

23. The configurable digital coherent demodulator system recited in Claim 22 further comprising:

a configurable extended and long code demodulator coupled to the configurable traffic channel demodulator.

24. The configurable digital coherent demodulator system recited in Claim 22 wherein the configurable parameter estimator provides a feed forward correction factor to the correction device.

25. The configurable digital coherent demodulator system recited in Claim 22 wherein the configurable parameter estimator has a configurable comparator circuit for receiving a configurable accumulator length.

26. The configurable digital coherent demodulator system recited in Claim 25 wherein the configurable correction device has an input for receiving a configurable delay value.

27. The configurable digital coherent demodulator system recited in Claim 25 wherein the configurable accumulator length input to the parameter estimator and the configurable delay value input to the correction device are proportional to each other.

28. A configurable receiver for a CDMA system, the receiver comprising:

an RF/IF stage for receiving an analog signal;

an analog-to-digital (A/D) converter for converting the analog signal to a digital signal;

a chip-matched filter for filtering the digital signal; and

at least one configurable digital coherent demodulator system having feed forward phase correction.

29. The configurable receiver recited in Claim 28 further comprising:

a plurality of configurable digital coherent demodulator systems having feed forward phase correction, the plurality of configurable digital coherent demodulators for demodulating multipath versions of a traffic signal.

30. The configurable receiver recited in Claim 28 wherein the at least one configurable digital coherent demodulator system includes a configurable parameter estimator for a pilot channel, the configurable parameter estimator having an input for receiving a configurable accumulator length.

31. The receiver recited in Claim 28 wherein the at least one configurable digital coherent demodulator system includes a configurable correction device having an input for receiving a configurable delay value

32. In a configurable parameter estimator, a method for estimating an error in a pilot channel, the method comprising the steps of:

a) receiving a first code demodulated sample and a second code-demodulated sample, each having an in-phase and a quadrature-phase component;

b) demodulating the first code demodulated sample and the second code demodulated sample with a pilot code sequence; and

c) performing an open-loop channel estimate on the first and second code demodulated samples using an open-loop channel estimator.

33. The method recited in Claim 32 further comprising the steps of:

d) filtering a first signal from the open-loop channel estimator at a first filter; and

e) filtering a second signal from the open-loop channel estimator at a second filter, wherein the first signal and the second signal represent an error correction signal.

34. The method recited in Claim 32 further comprising the steps of:

d) receiving a value specifying a variable pilot filter length using the first filter and the second filter.

35. The method recited in Claim 34 further comprising the steps of:

e) dumping a first sample from the first filter and a second sample from the second filter when the variable pilot filter length has been satisfied.

36. The method recited in Claim 32 wherein demodulating step b) further comprises the steps of:

b1) multiplying the first code demodulated sample with the pilot code sequence to create a first intermediate sequence; and

b2) multiplying the second code demodulated sample with the pilot code sequence to create a second intermediate sequence.

37. The method recited in Claim 36 wherein demodulating step b) further comprises- the steps of:

b3) providing an in-phase portion and a quadrature-phase portion of the first intermediate sequence at a first interface;

b4) providing an in-phase portion and a quadrature-phase portion of the second intermediate sequence at a second interface;

b5) adding the in-phase portion of the first intermediate sequence with the quadrature-phase portion of the second intermediate sequence at a first adder; and

b6) subtracting the quadrature-phase portion of the first intermediate sequence from the in-phase portion of the second intermediate sequence at a second adder.

38. A method of correcting the phase of a data signal using a configurable pilot assisted correction device, the method comprising the steps of:

a) receiving a demodulated output data sample;

b) receiving a phase correction signal; and

c) multiplying the demodulated output data sample with the phase correction signal at a multiplier to produce a phase-corrected data signal.

39. The method recited in Claim 38 further comprising the step of:

d) adding an in-phase portion of the phase-corrected data signal with a quadrature-phase portion of the phase-corrected data signal to produce a real signal.

40. The method recited in Claim 38 further comprising the step of:

d) delaying the demodulated output data sample at a delay circuit.

41. The method recited in Claim 40 further comprising the step of:

e) receiving a variable delay value using the pilot assisted correction device, the variable delay proportional to a pilot filter length in a pilot phase parameter estimator.

42. The method recited in Claim 38 wherein the phase correction signal is a feed forward signal.

43. A method of demodulating a user code from a received signal using a configurable user-code demodulator, the method comprising the steps of:

a) receiving a channel signal at an extended code/long code demodulator;

b) multiplying a first product code with an encoded data signal at a first multiply-logic device to produce a first code demodulated chip sequence;

c) summing the first code demodulated chip sequence at a first accumulator to produce a first code-demodulated sample;

d) multiplying a second product code with the encoded data signal at a second multiply-logic device to produce a second code demodulated chip sequence; and

e) summing the second code demodulated chip sequence at a second accumulator to produce a second code demodulated sample.

44. The method recited in Claim 43 further comprising the steps of:

f) receiving the first product code of a user code and an in-phase extended code; and

g) receiving the second product code of the user code and a quadrature-phase extended code.

45. The method recited in Claim 43 further comprising the steps of:

h) receiving a desired integration length value;

i) comparing the desired integration length value to a current integration length at a compare circuit; and

j) providing a dump enable signal to the first accumulator and the second accumulator if the current integration length satisfies the desired integration length.

46. The method recited in Claim 43 wherein multiplying steps b) and d) comprise the steps of:

multiplying a first m-ary component of a signal at a first complex multiply component; and

multiplying a second m-ary component of a signal at a second complex multiply device.

47. The method recited in Claim 43 wherein adding steps c) and e) comprise the steps of:

adding a first m-ary component of a signal at a first adder component; and

adding a second m-ary component of a signal at a second adder component.

48. A method of demodulating a traffic channel from a received signal at a configurable traffic channel demodulator, the method comprising the steps of:

a) receiving a first code demodulated sample and a second code demodulated sample;

b) receiving a traffic code sequence;

c) multiplying the traffic code sequence with the first code demodulated sample at a first multiplier to produce a first demodulated data sequence;

d) summing the first demodulated data sequence at a first accumulator to produce a first intermediate output data sample;

e) multiplying the traffic code with the second code demodulated sample at a second multiplier to produce a second code demodulated sequence; and

f) summing the second code demodulated sequence at a second accumulator to produce a second intermediate output data sample.

49. The method recited in Claim 48 further comprising the steps of:

g) adding an in-phase component of the first intermediate output data sample to a quadrature-phase component of the second intermediate output data sample at a first adder to obtain the quadrature-phase demodulated output data sample; and

h) subtracting the in-phase component of the second intermediate output data sample from a quadrature-phase component of the first intermediate output data sample at a second adder to obtain an in-phase demodulated output data sample.

50. The method recited in Claim 48 wherein steps a) and c) further comprise the following steps;

multiplying a first m-ary component of a signal at a first complex multiply component; and

multiplying a second m-ary component of the signal at a second complex multiply device.

51. The method recited in Claim 48 wherein summing steps b) and d) comprise the steps of:

adding a first m-ary component of the signal at a first adder component; and

adding a second m-ary component of the signal at a second adder component.

52. The method recited in Claim 48 further comprising the steps of:

g) receiving a desired integration length value;

h) comparing the desired integration length value to a current integration length at a compare circuit; and

i) providing a dump enable signal to the first accumulator and the second accumulator if the current integration length satisfies the desired integration length.

53. A method of demodulating a digital signal using a configurable digital coherent demodulator system, the method comprising the steps of:

a) receiving a baseline digital signal at a configurable traffic channel demodulator;

b) demodulating the baseline digital signal with a traffic code to obtain a traffic channel; and

c) receiving a feed forward phase error correction signal at a configurable correction device; and

d) multiplying the traffic channel by the feed forward phase error correction signal.

54. The method recited in Claim 53 further comprising the step of:

e) estimating a phase error correction signal of a pilot channel using a configurable parameter estimator.

55. The method recited in Claim 53 further comprising the steps of:

f) receiving a channel signal at a configurable extended code/long code demodulator; and

g) demodulating an extended code and a long code modulated signal from the complex channel signal using the configurable extended code/long code demodulator.

56. The method recited in Claim 54 further comprising the step of:

f) feeding forward the phase error correction signal to the configurable correction device.

57. The method recited in Claim 54 further comprising the step of:

f) receiving a configurable accumulator length at the configurable parameter estimator.

58. A method of processing data using a configurable CDMA receiver, the method comprising the steps of:

a) receiving an analog signal at an RF/IF stage;

b) converting the analog signal to a digital signal using an analog-to-digital (A/D) converter;

c) filtering the digital signal using a chip-matched filter to obtain a complex channel signal; and

d) processing the complex channel signal using a configurable demodulator system having a feed forward phase correction signal.

59. The method recited in Claim 58 further comprising the step of:

e) demodulating a user code sequence from the complex channel signal to produce a code demodulated sample; and

f) communicating the code demodulated sample to a plurality of configurable traffic demodulators.

60. The method recited in Claim 59 further comprising the step of:

g) demodulating a traffic code sequence from the code demodulated sample; and

h) communicating a demodulated output data sample to a plurality of configurable pilot assisted correction devices for each of a plurality of multipath channels.

61. The method recited in Claim 58 further comprising the step of:

e) feeding forward a digital phase correction signal from each of a plurality of configurable coherent demodulator systems to respectively correct a phase error in each of a plurality of a demodulated multipath data signals.

62. The method recited in Claim 58 wherein step d) includes the following sub steps:

d1) receiving a configurable pilot filter length at a configurable pilot channel estimator portion of the configurable demodulator system; and

d2) generating a digital error correction signal at an open loop phase estimator.

63. The method recited in Claim 58 further comprising the step of:

e) correcting a traffic channel via the feed forward digital phase correction signal using a configurable pilot assisted correction device.